Register No : _____

THE KAVERY ENGINEERING COLLEGE
(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Third Semester

Electrical and Electronics Engineering

EE3302 – Digital Logic Circuits

Regulations - 2021

Duration: 3 Hrs *Maximum: 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Convert $(1001)_2$ in to Decimal Number.	UN	1	2
2.	What is gray code?	RE	1	2
3.	Explain the list of advantages of K map method.	UN	2	2
4.	Simplify the expression Z=AB+AB'(A'C')'.	AP	2	2
5.	Write down the characteristics of JK flipflop.	UN	3	2
6.	What is FSM? List its two basic types.	RE	3	2
7.	What are the two types of asynchronous sequential circuits?	RE	4	2
8.	Define PROM.	RE	4	2
9.	Describe RTL in HDL with an example.	UN	5	2
10.	List the purpose of test bench.	RE	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Explain TTL logic in detail along with their types.	UN	1	13
			Or			
	b	i	Write short notes RTL and DTL.	RE	1	6
		ii	Design two input NOR GATE.	AP	1	7
12.	a		Apply K-map and simplify the following. y = C'(A'B'D'+ D)+ AB'C +D'.	AP	2	13
			Or			
	b	i	Design a 4-bit Binary gray code converter using logic gates.	AP	2	9
		ii	Give the applications of multiplexer and decoder.	RE	2	4
13.	a	i	Explain Moore and Mealy models with the help of block diagrams.	UN	3	7
		ii	Design a 5-bit ring counter and mention its applications.	UN	3	6
			Or			
	b		What is meant by a Flip Flop? Write the characteristics equation, characteristics table and draw logic of SR, JK and D flipflops.	AP	3	13

14.	a		Differentiate PAL and PLA implementations with the help of the same example: F_2 (a, b, c) = Σ(0, 1, 3, 4, 6, 7).	AP	4	13
			Or			
	b	i	Explain cycles and races in asynchronous sequential circuits.	AP	4	7
		ii	What are transition table and flow table? Give suitable examples.	UN	4	6
15.	a		Explain in detail the RTL design procedure with an example.	UN	5	13
			Or			
	b		Write the VHDL code to realize a 4-bit parallel binary adder with structural modeling and write the test bench to verify its functionality.	AP	5	13

*PART – C (Marks 1*15 = 15)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
16.	a		Design and explain 3 bit shift register. Also give its truth table with its input and output waveform.	AN	EV	15
			Or			
	b		Draw the circuit of CMOS AND gate and explain its operation. Also implement using VHDL.	AN	5	15